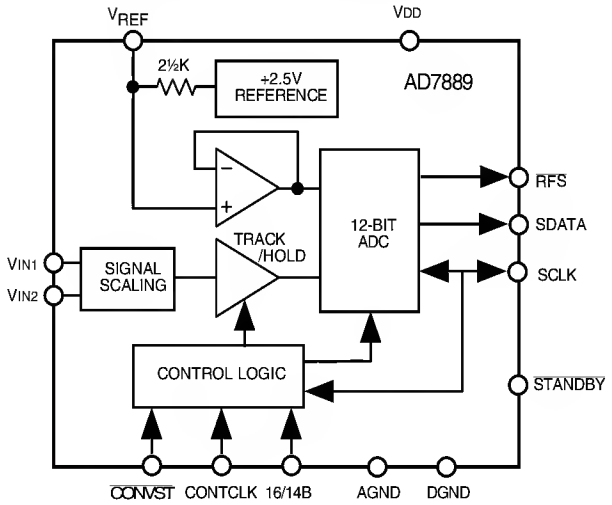
LC²MOS Single Supply, 12-Bit 600 kSPS ADC

Preliminary Technical Information — AD7889

FEATURES

Fast 12-Bit ADC with 1.4 µs Conversion Time
Up to 600 kSPS Throughput Rate (Mode A)
Single Supply Operation
On-Chip Track/Hold Amplifier
Selection of Input Ranges:
±10 V or ±5 V for AD7889-1
0 V to +2.5 V or 0V to+5 V for AD7889-2
±2.5 V for AD7889-3
High Speed Serial Interface
Low Power, 60 mW typ

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7889 is a high speed, low power, 12-bit A/D converter that operates from a single +5 V supply. The part contains a successive approximation ADC, an on-chip track/hold amplifier, an internal +2.5 V reference and on-chip versatile interface structures that allows serial communication to a microprocessor in a variety of operating modes. The part accepts an analog input range of ±10 V or ±5 V (AD7889-1), 0 V to +2.5 V or 0 V to +5V (AD7889-2) and ±2.5 V (AD7889-3). Overvoltage protection on the analog inputs for the AD7889-1 and AD7889-3 allows the input voltage to go to ±17 V or ±7 V respectively without damaging the ports.

The AD7889 offers a choice of serial interface modes which allows direct connection to the serial ports of microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7889 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. It is available in a 16-pin, SSOP.

PRODUCT HIGHLIGHTS

1. The AD7889 features a conversion time of 1.4µs (Mode A) and a track/hold acquisition time of 300ns. This allows a throughput rate for the part up to 600 kSPS. Modes C and D can be used to allow a throughput rate of 500kSPS.
2. The AD7889 operates from a single +5 V supply and consumes 60 mW typ making it ideal for low power and portable applications.
3. The part offers a high speed, serial interface for easy connection to microprocessors, microcontrollers and digital signal processors.

REV. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD7889–SPECIFICATIONS (V_{DD} = +5 V ±5%, AGND = DGND = 0 V, REF IN = +2.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version[2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					
AD7889-1, AD7889-2					f_{IN} = 100 kHz. f_{SAMPLE} = 500 kSPS
Signal to (Noise + Distortion) Ratio[3]	70	70	70	dB min	
Total Harmonic Distortion[3]	–80	–80	–78	dB max	
Peak Harmonic or Spurious Noise[3]	–81	–81	–79	dB max	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–80	–80	–78	dB max	
3rd Order Terms	–80	–80	–78	dB max	
AD7889-3					f_{IN} = 100 kHz. f_{SAMPLE} = 600 kSPS
Signal to (Noise + Distortion) Ratio[3]	70	70		dB min	
Total Harmonic Distortion[3]	–78	–78		dB max	
Peak Harmonic or Spurious Noise[3]	–79	–79		dB max	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–78	–78		dB max	
3rd Order Terms	–78	–78		dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]		±1	±1	LSB max	
Differential Nonlinearity[3]		±1	±1	LSB max	
Positive Full-Scale Error[3]	±4	±4	±5	LSB max	
AD7889-1					
Negative Full-Scale Error[3]	±4	±4	±5	LSB max	
Bipolar Zero Error[3]	±3	±2	±3	LSB max	
AD7889-3					
Negative Full-Scale Error[3]	±4	±4		LSB max	
Bipolar Zero Error[3]	±4	±3		LSB max	
AD7889-2 Only					
Unipolar Offset Error[3]	±4	±3	±4	LSB max	
ANALOG INPUT					
AD7889-1					
Input Voltage Range	±10	±10	±10	Volts	Input Applied to V_{IN1} with V_{IN2} Grounded
Input Voltage Range	±5	±5	±5	Volts	Input Applied to V_{IN1} and V_{IN2}
Input Resistance	25	25	25	kΩ min	Input Applied to V_{IN1} with V_{IN2} Grounded
AD7889-2					
Input Voltage Range on V_{IN1}	0 to +5	0 to +5	0 to +5	Volts	Input Applied to V_{IN1} with V_{IN2} Grounded
Input Voltage Range on V_{IN1}	0 to +2.5	0 to +2.5	0 to +2.5	Volts	Input Applied to V_{IN1} and V_{IN2}
Input Current	10	10	50	nA max	
AD7889-3					
Input Voltage Range on V_{IN1}	±2.5	±2.5		Volts	Input Applied to V_{IN1}
Input Resistance	2	2		kΩ min	
REFERENCE OUTPUT/INPUT					
VREF Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[4]	10	10	10	pF max	
VREF Output Voltage	2.5	2.5	2.5	V nom	
VREF Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
VREF Temperature Coefficient	25	25	25	ppm/°C typ	
VREF Output Impedance	5.5	5.5	5.5	kΩ nom	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	

Parameter	A Versions[1]	B Versions	S Version[2]	Units	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Capacitance[4]	15	15	15	pF max	
Output Coding					
AD7889-1 and AD7889-3	2s Complement				
AD7889-2	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	1.4	1.4		µs max	Mode A
Conversion Time	1.6	1.6		µs max	Modes C and D
Conversion Time	2.4	2.4		µs max	Mode B
Track/Hold Acquisition Time[3]	0.3	0.3		µs max	All Modes
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}[5]					
Normal Operation	18	18	19	mA max	
Standby Mode[6]					
AD7889-1, AD7889-2	250	250	15	µA typ	
AD7889-3	40	40		µA max	
Power Dissipation[5]					
Normal Operation	90	90	95	mW max	V_{DD} = +5 V. Typically 60 mW
Standby Mode[6]					
AD7889-1, AD7889-2	1.25	1.25	0.075	mW typ	
AD7889-3	200	200		µW max	V_{DD} = +5 V. Typically 50 µW

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.
[2]S Version available on AD7889-1 and AD7889-2 only.
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
[5]These normal mode and standby mode currents are achieved with resistors (in the range 10 kΩ to 100 kΩ) to either DGND or V_{DD} on Pins x, x, x and x.
[6]A conversion should not be initiated on the part within 30 µs of exiting standby mode.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND
AD7889-1 ..... ±17 V
AD7889-2 ..... +7 V
AD7889-3 ..... ±7 V
Reference Input Voltage to AGND .. –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Versions) ..... –40°C to +85°C
Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
SSOP Package, Power Dissipation. ..... 450 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ±5%, AGND = DGND = 0 V, REF IN = +2.5 V)

Parameter	A, B Versions	S Version	Units	Test Conditions/Comments
t_{CONV}	1.4		µs max	Conversion Time for AD7889 (Mode A)
	1.6	1.6	µs max	Conversion Time for AD7889 (Modes C &D)
t_{ACQ}	300		ns min	Acquisition Time for AD7889
Serial Interface				
t_1[3]	20	20	ns min	SCLK Rising Edge to Data Valid Hold Time
t_2[3]	30	35	ns min	RFS Low to SCLK Falling Edge Setup Time
t_3	25	25	ns min	SCLK High Pulse Width
t_4	25	25	ns min	SCLK Low Pulse Width
t_5	XX	XX	ns min	CONVST High to SCLK Falling Edge
t_6	20	20	ns min	SCLK Rising Edge to RFS Rinsing Edge
t_8	25	25	ns max	SCLK High Pulse Width (Mode B)
t_9	25	25	ns min	SCLK Low Pulse Width (Mode B)
t_{10}	XX	XX	ns min	CONVST High to RFS Falling Edge

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.
[2]See Figures 2a - 2d.
[3]Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

Specifications subject to change without notice.

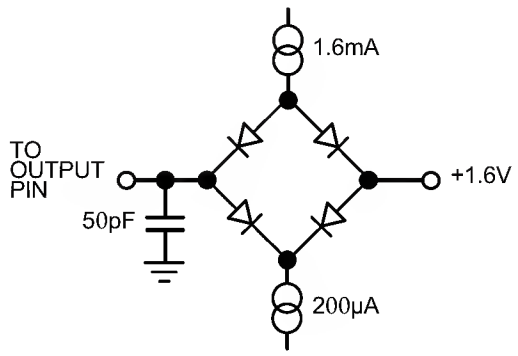


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7889 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

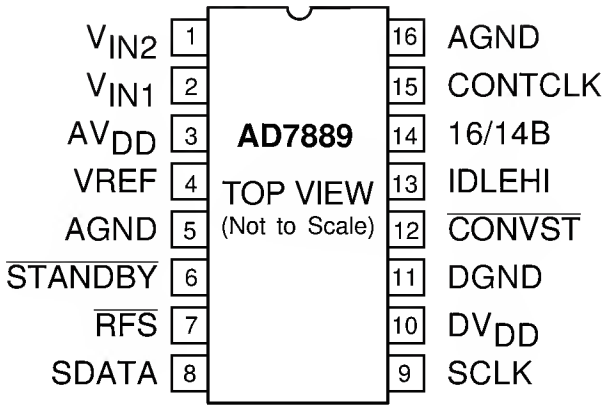
ORDERING GUIDE

Model	Input Range	Sample Rate	Relative Accuracy	Temperature Range	Package Option[1]
AD7889ARS-1	±5 V or ±10 V	600 kSPS		–40°C to +85°C	RS-16
AD7889BRS-1	±5 V or ±10 V	600 kSPS	±1 LSB	–40°C to +85°C	RS-16
AD7889ARS-2	0 V to 2.5 V or 0 V to 5 V	500 kSPS		–40°C to +85°C	RS-16
AD7889ARS-3	±2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	RS-16
EVAL-AD7889-1CB[2]	Evaluation Board				
EVAL-AD7889-2CB[2]	Evaluation Board				
EVAL-AD7889-3CB[2]	Evaluation Board				
EVAL-CONTROL BOARD[3]	Controller Board				

NOTES
[1]R S= SSOP.
[2]These boards can be used as stand-alone evaluation boards or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices' evaluation boards ending in the CB designators.

PIN CONFIGURATION

SSOP



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	V_{IN2}	Analog Input 2. For the AD7889-1, this input either connects to AGND or to V_{IN1} to determine the analog input voltage range. With V_{IN2} connected to AGND on the AD7889-1, the analog input range at the V_{IN1} input is ±10 V. With V_{IN2} connected to V_{IN1} on the AD7889-1, the analog input range to the part is ±5 V. With V_{IN2} connected to AGND on the AD7889-2, the analog input range at the V_{IN1} input is 0 V to +5 V. With V_{IN2} connected to V_{IN1} on the AD7889-2, the analog input range to the part is 0 V to +2.5 V. For theAD7889-3, this input can be left unconnected but must not be connected to a potential other than AGND.
2	V_{IN1}	Analog Input 1. The analog input voltage to be converted by the AD7889 is applied to this input. For the AD7889-1, the input voltage range is either ±5 V or ±10 V depending on where the V_{IN2} input is connected. For the AD7889-2, the voltage range on the V_{IN1} input is 0 V to +2.5 V or 0 V to +5 V with respect to the voltage appearing at the V_{IN2} input. For the AD7889-3, the voltage range on the V_{IN1} input is ±2.5 V.
3	AV_{DD}	Positive supply voltage, +5V ±5%.
4	VREF	Voltage Reference Input. An external reference source should be connected to this pin to provide the reference voltage for the AD7889s conversion process. The nominal reference voltage for the AD7889 is 2.5V.
5	AGND	Analog Ground. Ground reference for analog circuitry.
6	STANDBY	Standby Input. Logic Input. With this input at a logic high, the part is in its normal operating mode; with this input at a logic low the part is placed in its standby or power-down mode, which reduces power comsumption to 5mW typical.
7	RFS	Receive Frame Synchronization. Digital Output. This signal goes low for the duration of valid output data.
8	SDATA	Serial Data. Logic Output. Serial data is provided on this pin when RFS is low.
9	SCLK	Serial Clock. Logic Input/Output. This pin is used to clock serial data from the AD7889. The pin can be either an input or an output depending on which interface mode is used. The interface mode is selected by the 16/14B and CONTCLK pins.
10	DV_{DD}	Positive supply voltage for digital logic, +5 V ±5%.
11	DGND	Digital Ground. Ground reference for digital circuitry.
12	CONVST	Convert Start. Logic Input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion.
13	IDLEHI	Idle High. Level triggered input. This input controls the idle state of the serial clock. With the input high, data should be latched on the falling edge of SCLK. With the input low, data should be latched on the rising edge of SCLK.
14	16/14B	16 Clock/14 Clock. Digital Input. This input determines how many clock cycles will be used to complete a conversion. If the input is high the AD7889 will take 16 clock cycles to complete a conversion. If the input is low the AD7889 will take 14 clock cycles to complete a conversion.
15	CONTCLK	Continuous Clock. Digital Input. This input tells the AD7889 whether a continuous or burst serial clock is being used. When the input is high the AD7889 expects to receive a continuous serial clock. When the input is low the AD7889 expects to receive either a burst of 16 or 14 serial clocks (depending on the state of 16/14B).
16	AGND	Analog Ground. Ground reference for analog circuitry.

TERMINOLOGY

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion)
ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (Noise + Distortion) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7889, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where *m*, *n* = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither *m* nor *n* are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7889 is tested using two input frequencies away from the bottom end of the input bandwidth. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error (AD7889-1)
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal 4 × REF IN – 3/2 LSB (±10 V range) or 2 × REF IN – 3/2 LSB (±5 V range) after the bipolar zero
error has been adjusted out.

Positive Full-Scale Error (AD7889-2)
This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal REF IN – 3/2 LSB (0V to2.5V range) or 2 × REF IN – 3/2 LSB (0V to 5V range) after the unipolar offset error has been adjusted out.

Positive Full-Scale Error (AD7889-3)
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (REF IN – 3/2 LSB) after the bipolar zero error has been adjusted out.

Bipolar Zero Error (AD7889-1, AD7889-3)
This is the deviation of the midscale transition (all 1s to all 0s) from the ideal (AGND – 1/2 LSB).

Unipolar Offset Error (AD7889-2)
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal (AGND + 1/2 LSB).

Negative Full-Scale Error (AD7889-1)
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal –4 × REF IN + 1/2 LSB (±10 V range) or –2× REF IN + 1/2 LSB (±5 V range) after bipolar zero error has been adjusted out.

Negative Full-Scale Error (AD7889-3)
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal – REF IN + 1/2 LSB after bipolar zero error has been adjusted out.

Track/Hold Acquisition Time
Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the V_{IN} input of the AD7889. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

CIRCUIT DESCRIPTION

The AD7889 is a fast, 12-bit single supply A/D converter. It provides the user with signal scaling, track/hold, reference, A/D converter and versatile interface logic functions on a single chip. The signal scaling on the AD7889-1 allows the part to handle either ±5 V or ±10 V input signals while operating from a single +5 V supply. The AD7889-2 handles either a 0 V to +2.5 V or 0 V to +5.0 V analog input range, while signal scaling on the AD7889-3 allows it to handle ±2.5 V input signals when operating from a single supply. The part requires a +2.5 V reference which can be provided from the part's own internal reference or from an external reference source.

Conversion is initiated on the AD7889 by pulsing the CONVST input. On the rising edge of CONVST, the track/hold goes from track mode to hold mode and the conversion sequence is started. At the end of conversion , the track/hold returns to tracking mode and the acquisition time begins. Conversion times for the part are 1.4μs(Mode A) and 1.6 μs (Modes B-D) The track/hold acquisition time is 300 ns. This allows the AD7889 to operate at throughput rates up to 600 kSPS.

Track/Hold Section

The track/hold amplifier on the AD7889 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 600 kHz (i.e., the track/hold can handle input frequencies in excess of 300 kHz).

The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 300 ns. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode on the rising edge of CONVST. The aperture time for the track/hold (i.e., the delay time between the external CONVST signal and the track/hold actually going into hold) is typically 15 ns. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point.

Reference Section

The AD7889 contains a single reference pin, labelled VREF, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7889's transfer function and will add to the specified full-scale errors on the part. On the AD7889-1 and AD7889-3, it will also result in an offset error injected in the attenuator stage.

The AD7889 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7889, simply connect a 0.1 μF disc ceramic capacitor from the VREF pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7889, it should be buffered as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 5.5 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±25 mV.

If the application requires a reference with a tighter tolerance or the AD7889 needs to be used with a system reference, then the user has the option of connecting an external reference to this VREF pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current is ±100 μA. Suitable reference sources for the AD7889 include the AD680, AD780 and REF43 precision +2.5 V references.

INTERFACING

The part has a versatile serial 3 wire interface with four modes of operation. The modes are selected using the CONTCLK and 16/14B pins. The serial interface can be set up to use either a continuous or burst clock. With CONTCLK at a logic 1 the AD7889 expects a continuous serial clock to be provided. With CONTCLK at a logic 0 the AD7889 expects a burst serial clock to be provided. Table I shows the interface modes available.

Table I. AD7889 Interface Modes

Interface Mode	16/14B	CONTCLK
Mode A	0	0
Mode B	0	1
Mode C	1	0
Mode D	1	1

Figures 2a-2d show the timing diagrams for reading from the AD7889 in the various serial interface modes. RFS is driven low as the AD7889 outputs the data.

MODE A Description.

The AD7889 can be used in Mode A by connecting CONTCLK and 16/14B to logic 0. In this mode the AD7889 provides a burst SCLK. The conversion is initiated by pulsing CONVST. 14 SCLK pulses are provided to output the conversion result. After the first two rising edges of SLCK (assuming IDLEHI = 1) the RFS signal is asserted. The conversion result is available on the next 12 falling SCLK edges.

MODE B Description.

The AD7889 can be used in Mode B by connecting CONTCLK to logic 1 and 16/14B to logic 0. In this mode the AD7889 expects a continuous SCLK to be provided.The conversion is initiated by pulsing CONVST. The RFS signal is asserted after the first rising edge of the SCLK following a CONVST.The following 14 clock cycles contain the conversion result with the first two bits being don't cares.The 15th rising edge after the CONVST will bring the RFS back high.

MODE C Description.

The AD7889 can be used in Mode C by connecting CONTCLK to logic 0 and 16/14B to logic 1. In this mode the AD7889 expects a burst SCLK to be provided.The conversion is initiated by pulsing CONVST. The RFS signal is then asserted and 16 serial clocks should be provided. The conversion result will be valid on the falling edges of the 16 clock cycles (assuming IDLEHI = 1). When the clock returns to its idle state (dependent on IDLEHI) the RFS will return high.

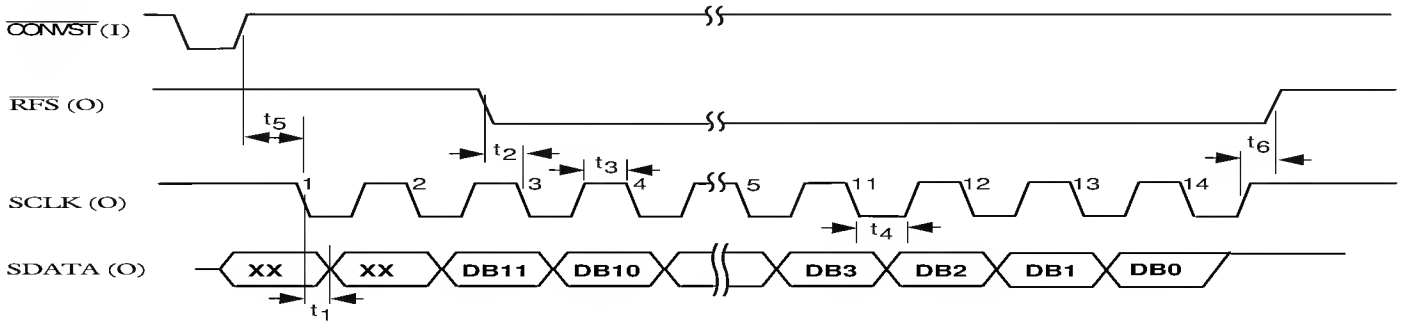


Figure 3a. Mode A Timing Diagram (IDLEHI=1)

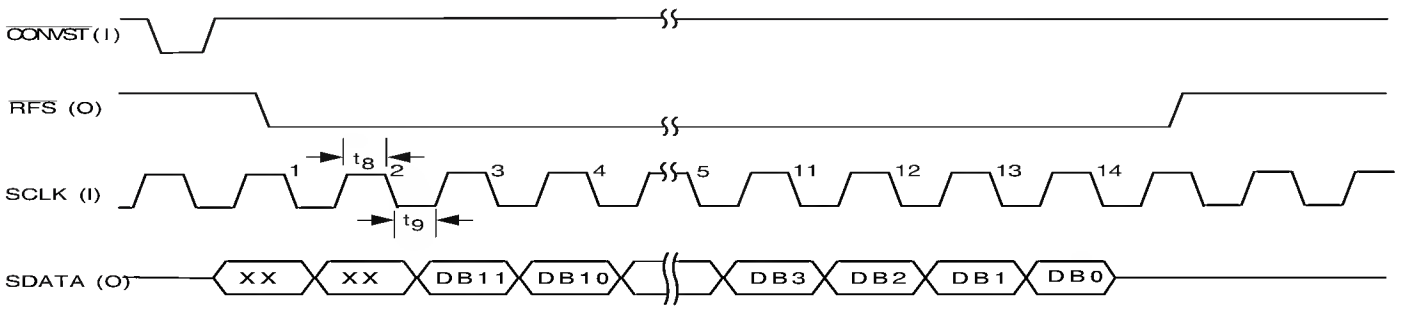


Figure 3b. Mode B Timing Diagram (IDLEHI=1)

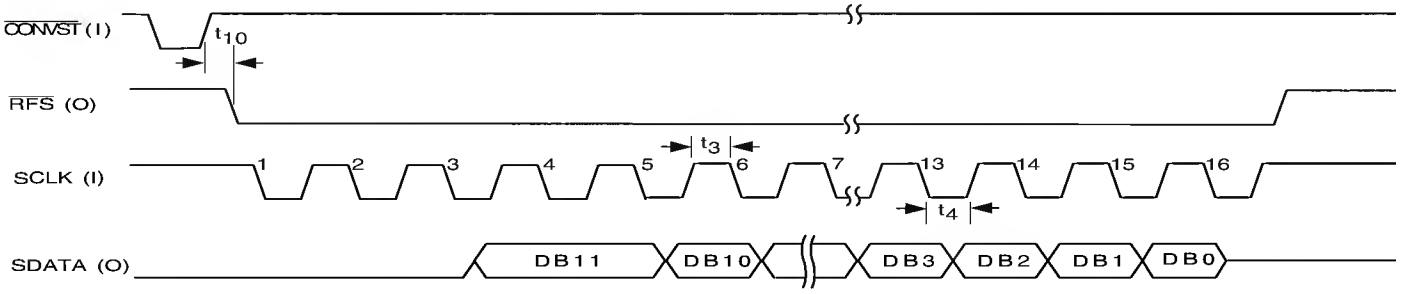


Figure 3c. Mode C Timing Diagram (IDLEHI=1)

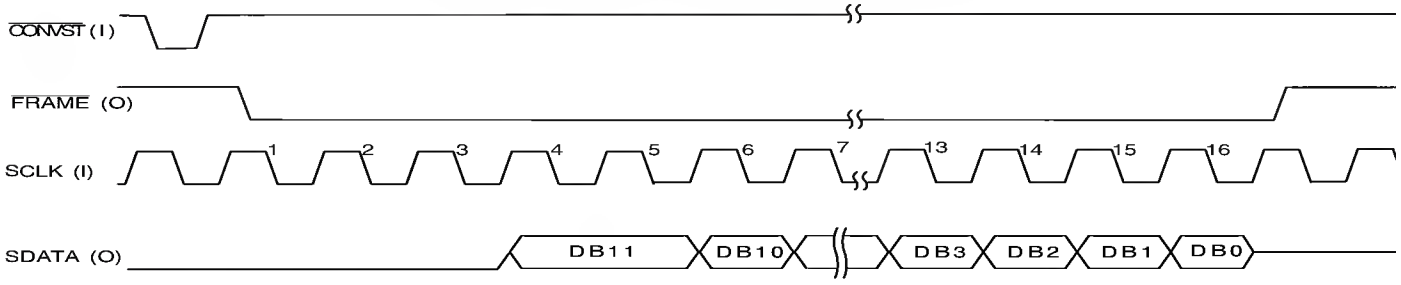


Figure 3d. Mode D Timing Diagram (IDLEHI=1)

MODE D Description.

The AD7889 can be used in Mode D by connecting CONTCLK and 16/14B to logic 1. In this mode the AD7889 expects a continuous SCLK to be provided.The conversion is initiated by pulsing CONVST. The first rising edge of the SCLK following the CONVST causes the RFS to be asserted. The conversion result is available on the next 16 falling edges of SCLK (assuming IDLEHI = 1). The RFS returns back high on the rising edge following the last bit of data.

Analog Input Section

The AD7889 is offered as three part types allowing for five different analog input voltage ranges. The AD7889-1 handles either ±5 V or ±10 V input voltage ranges. The AD7889-2 handles either 0 V to +2.5 V or 0 V to +5 V input voltage ranges while the AD7889-3 handles an input range of ±2.5 V.

AD7889-1

Figure 3 shows the analog input section for the AD7889-1. The analog input range is pin-strappable (using V_{IN2}) for either ±5 V or ±10 V on the V_{IN1} input. With V_{IN2} connected to AGND, the input range on V_{IN1} is ±10 V, and the input resistance on V_{IN1} is 25 kΩ nominal. With V_{IN2} connected to V_{IN1}, the input range on V_{IN1} is ±5 V, and the input resistance on V_{IN1} is 15kΩ nominal. As a result, the V_{IN1} and V_{IN2} inputs should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to ±17 V without damaging the AD7889-1.

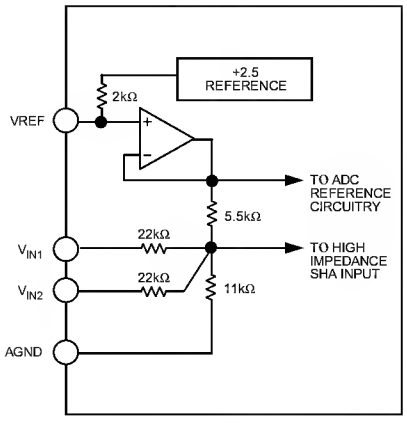


Figure 3. AD7889-1 Analog Input Structure

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is 2s complement binary with 1 LSB = FSR/4096 = 20 V/4096 = 4.88 mV for the ±10 V range and 1 LSB = FSR/4096 = 10 V/4096 = 2.44 mV for the ±5 V range. The ideal input/output transfer function for the AD7889-1 is shown in Table II.

Table II. Ideal Input/Output Code Table for the AD7889-1

Analog Input	Digital Output Code Transition
+FSR/2 – 3/2 LSB[1, 2] (9.99268 or 4.99634)[3]	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSBs (9.98779 or 4.99390)	011 . . . 101 to 011 . . . 110
+FSR/2 – 7/2 LSBs (9.98291 or 4.99146)	011 . . . 100 to 011 . . . 101
AGND + 3/2 LSB (0.00732 or 0.00366)	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB (0.00244 or 0.00122)	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB (–0.00244 or –0.00122)	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB (–0.00732 or –0.00366)	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSB (–9.98779 or –4.99390)	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSB (–9.99268 or –4.99634)	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB (–9.99756 or –4.99878)	100 . . . 000 to 100 . . . 001

NOTES

[1]FSR is full-scale range and VREF = +2.5 V, is 20 V for the ±10 V range and 10 V for the ±5 V range.

[2]1 LSB = FSR/4096 = 4.88 mV (±10 V range) and 2.44 mV (±5 V range) with VREF = +2.5 V.

[3]±10 V range or ±5 V range.

AD7889-2

Figure 4 shows the analog input section for the AD7889-2. The analog input range is pin-strappable (using V_{IN2}) for either 0 V to +2.5 V or 0V to +5 V. With V_{IN2} connected to AGND, the input range on V_{IN1} is 0 V to +5 V, and the input resistance on V_{IN1} is 11kΩ nominal. With V_{IN2} connected to V_{IN1}, the input range on V_{IN1} is 0 V to 2.5 V, and the input resistance on V_{IN1} is 2.75kΩ nominal. As a result, the V_{IN1} and V_{IN2} inputs should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to +7 V without damaging the AD7889-2.

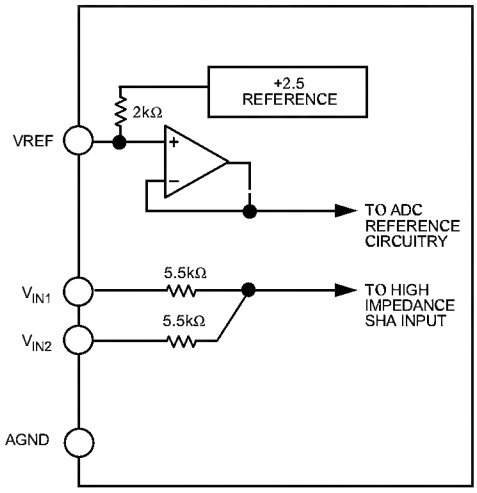


Figure 4. AD7889-2 Analog Input Structure

Once again, the designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is straight (natural) binary with 1 LSB = FSR/4096 = 2.5 V/4096 = 0.61 mV, for the 0 V to 2.5V range and 1 LSB = FSR/4096 = 5 V/4096 = 1.22 mV, for the 0 V to 5V range. The ideal input/output transfer function for the AD7889-2 is shown in Table III.

Table III. Ideal Input/Output Code Table for the AD7889-2

Analog Input	Digital Output Code Transition
+FSR – 3/2 LSB[1, 2] (4.998169 V)	111 . . . 110 to 111 . . . 111
+FSR – 5/2 LSBs (4.996948 V)	111 . . . 110 to 111 . . . 110
+FSR – 7/2 LSBs (4.995728 V)	111 . . . 100 to 111 . . . 101
AGND + 5/2 LSB (0.003052 V)	000 . . . 010 to 010 . . . 011
AGND + 3/2 LSB (0.01832 V)	000 . . . 001 to 001 . . . 010
AGND + 1/2 LSB (0.000610 V)	000 . . . 000 to 000 . . . 001
+FSR – 3/2 LSB[2, 3] (2.499084 V)	111 . . . 110 to 111 . . . 111
+FSR – 5/2 LSBs (2.498474 V)	111 . . . 110 to 111 . . . 110
+FSR – 7/2 LSBs (2.497864 V)	111 . . . 100 to 111 . . . 101
AGND + 5/2 LSB (0.001526 V)	000 . . . 010 to 010 . . . 011
AGND + 3/2 LSB (0.00916 V)	000 . . . 001 to 001 . . . 010
AGND + 1/2 LSB (0.000305 V)	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 5 V with VREF = +2.5 V.
[2]1 LSB = FSR/4096 = 1.22 mV (0V to +5V range) and 0.61 mV (0V to 2.5V range) with VREF = +2.5 V.
[3] FSR is full-scale range and is 2.5V with VREF= +2.5 V.

AD7889-3

Figure 5 shows the analog input section for the AD7889-3. The analog input range is ±2.5 V on the V_{IN1} input. The V_{IN2} input can be left unconnected but if it is connected to a potential then that potential must be AGND. The input resistance on the V_{IN1} is 2.75 kΩ nominal. As a result, the V_{IN1} input should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to ±7 V without damaging the AD7889-3.

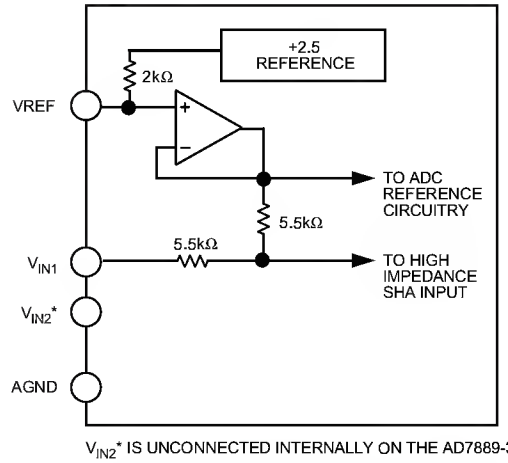


Figure 5. AD7889-3 Analog Input Structure

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is 2s complement binary with 1 LSB = FSR/4096 = 5 V/4096 = 1.22 mV with VREF = +2.5 V. The ideal input/output transfer function for the AD7889-3 is shown in Table IV.

Table IV. Ideal Input/Output Code Table for the AD7889-3

Analog Input	Digital Output Code Transition
+FSR/2 – 3/2 LSB[1, 2] (2.49817)	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSBs (2.49695)	011 . . . 110 to 011 . . . 110
+FSR/2 – 7/2 LSBs (2.49573)	011 . . . 110 to 011 . . . 101
AGND + 3/2 LSB (0.00183)	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB (0.00061)	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB (–0.00061)	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB (–0.00183)	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSB (–2.49695)	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSB (–2.49817)	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB (–2.49939)	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and is 5 V with VREF = +2.5 V.
[2]1 LSB = FSR/4096 = 1.22 mV with VREF = +2.5 V.

MICROPROCESSOR INTERFACING

The AD7889 features a high speed serial interfaces with four modes of operation, allowing considerable flexibility in interfacing to microprocessor systems.

Figures 6, 7 and 8 show some typical interface circuits between the AD7889 and popular DSP processors. The CONVST signal can be generated by a flag pin from the DSP or by external hardware controlled by a timer.

AD7889 to ADSP-21XX Interface

Figure 6 shows a serial interface between the AD7889 and the ADSP-21XX family of DSP processors. TheAD7889 is operating in Mode A (maximum throughput) and the RFS and SCLK signals are inputs to the DSP. The flag pin FL0 (controlled by an internal timer routine) is used to provide the CONVST. Pulsing CONVST starts conversion and data is provided on the subsequent clock edges.

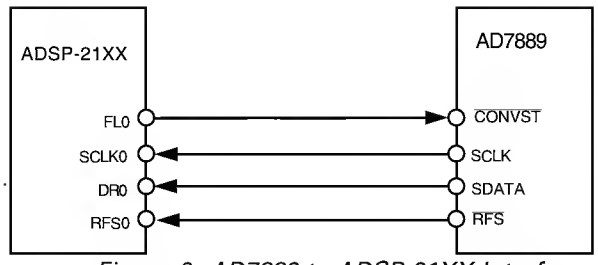


Figure 6. AD7889 to ADSP-21XX Interface

AD7889 to TMS320C20 Interface
Figure 7 shows the interface between the AD7889 (again in Mode A) and the TMS320C20 DSP processor. Here a timer is used to generate the CONVSTpulse to ensure equidistant sampling. For the TMS320C20 the CLKX, CLKR, FSX and FSR should all be configured as inputs. The CLKX and CLKR should be connected together as should the FSX and FSR.

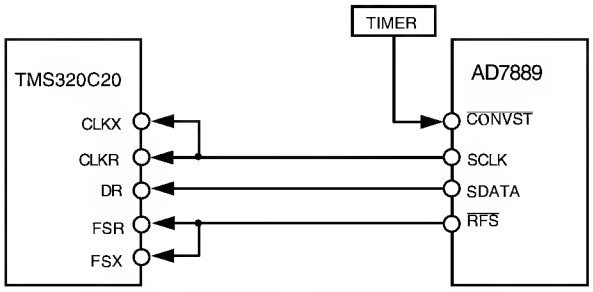


Figure7. AD7889 to TMS320C20 Interface

AD7889 to DSP56000 Interface
Figure 8 shows the interface between the AD7889 and the DSP56000 DSP processor.Again a timer is used to start conversion and the data is clocked on the subsuquent clock edges.

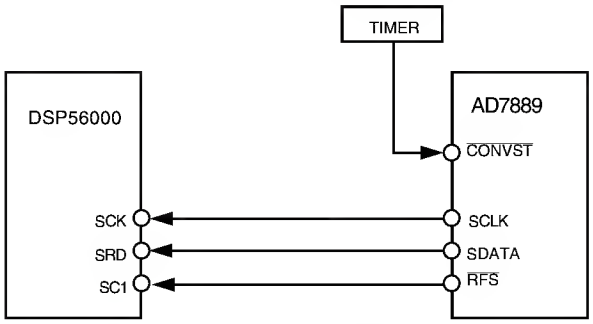


Figure 8. AD7889 to DSP56000 Interface

Grounding and Layout
The analog and digital supplies to the AD7889 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The part exhibits good immunity to noise on the supplies but care must still be taken with regard to grounding and layout especially when using switching mode supplies.

The printed circuit board which houses the AD7889 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7889 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7889. If the AD7889 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7889.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7889 to avoid noise coupling. The power supply lines to the AD7889 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF disc ceramic capacitors to DGND.In systems where a common supply is used to drive both the AV_{DD} and DV_{DD} of the AD7889, it is recommended that the systems AVDD supply is used. In this case there should be a 10Ω resistor between the AV_{DD} pin and DV_{DD} pin. This supply should have the recommended analog supply decoupling capacitors between the V_{DD} pin of the AD7889 and AGND and the recommended digital supply decoupling capacitor between the V_{DD} pin of the AD7889 and DGND.

Evaluating the AD7889 Performance
The recommended layout for the AD7889 is outlined in the evaluation board for the AD7889. The evaluation board package includes a fully assembled and tested evaluation board, documentation and software for controlling the board from a PC using the EVAL-CONTROL BOARD. The EVAL-CONTROL BOARD can be used in conjunction with the AD7889 evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator. Using the EVAL-CONTROL BOARD with the AD7889 evaluation board allows the user to evaluate the ac and dc performance of the AD7889 on a PC.

The software provided with the evaluation board allows the user to perform ac (Fast Fourier Transform) and dc (histogram of codes) tests on the AD7889. The evaluation board can also be used in a stand-alone fashion without the EVAL-CONTROL BOARD but in this case, the user has to write their own software to evaluate the part. There are three versions of the evaluation board available, one for the AD7889-1, one for the AD7889-2 and one for the AD7889-3. The order numbers for the evaulation boards are EVAL-AD7889-1CB, EVAL-AD7889-2CB and EVAL-AD7889-3CB.